4-state anti-ferroelectric random access memory

Melvin M. Vopson, Xiaoli Tan

Abstract — Ferroelectric random access memory (FRAM) is a 2-state non-volatile memory, in which information is digitally encoded using switchable remanent polarization states within a ferroelectric thin film capacitor. Here we propose a novel non-volatile memory based on anti-ferroelectric polycrystalline ceramics, termed anti-ferroelectric random access memory (AFRAM). The AFRAM memory cell architecture is similar to FRAM, but it requires a more complex operation protocol. Our initial experimental demonstration of the memory effect in anti-ferroelectric ceramic shows, remarkably, that the AFRAM technology encodes data in both ferroelectric sublattices of the anti-ferroelectric medium. This results in a 4-state non-volatile memory capable of storing 2 digital bits simultaneously, unlike the FRAM technology that has 2-memory states and it is capable to store 1 digital bit per cell.

Index Terms—Ferroelectric devices, Memory architecture, Nonvolatile memory, Random access memory

I. INTRODUCTION

Random access memory (RAM) is a key component in computer memories and consumer electronics. Volatile RAM means that the memory chip stores information as long as electric power is supplied to it, while the non-volatile RAM can store data without power [1]. Ferroelectric random access memories, known as FRAM or FeRAM, are non-volatile RAMs [2-6] that utilize the properties of ferroelectric materials to store digital data. Each cell stores binary "0" and "1" states as one of two possible electric remanent polarization states. The main benefits of FRAM memories against competitor technologies are their low power consumption, ultra-fast data accesses times and "read / write" endurance of 10 trillion (= 10^{13} "read / write" cycles) [fujitsu.com]. However, FRAM chips are lagging behind in terms of data storage capacity. The largest commercially available FRAM memory chips today are 4Mb. They can operate at 5V or below, with typical operation voltage of 1.5 V in chips using $Pb(Zr_xTi_{1-x})O_3$ (PZT) capacitors and < 1 V in chips using $SrBi_2Ta_2O_9$ (SBT) capacitors. FRAM chips are utilized in various applications where the memory size is not a critical requirement, including RF-ID chips, security tags, smart meters, failure analysis in industrial machines, car navigation systems and other consumer electronics [7,8]. In order to be competitive with other non-volatile RAM technologies, future FRAM must achieve high data storage density, which means shrinking the cell size without reducing the stored charge. Various ideas are currently under development, including the

fabrication of 3D ferroelectric capacitor structures [9]. In this paper an alternative solution is proposed: the use of anti-ferroelectric capacitors for non-volatile 4-state anti-ferroelectric random access memory, termed here AFRAM.

II. AFRAM MEMORY CELL CONCEPT AND OPERATION

The AFRAM memory concept proposed in this article was prompted by the following question: *Could digital data be encoded in each induced ferroelectric sublattice of the anti-ferroelectric material?* Let us examine this concept in detail. Fig. 1 (A) shows a typical polarization versus electric field / voltage response of an anti-ferroelectric material. Unlike ferroelectrics, which display a single hysteresis loop, the anti-ferroelectric materials display a double hysteresis loop. Each hysteresis loop represents the response of the induced ferroelectric phase of one of the two ferroelectric sublattices coexisting within the anti-ferroelectric. We shall refer to the two induced ferroelectric phases simply as Sublattice 1 – FE1 and Sublattice 2 – FE2. Hence, the positive hysteresis loop in Fig. 1 (A) corresponds to FE1, and the negative hysteresis loop corresponds to FE2. Let $+/-V_s$ be the polarization saturation voltage. Assuming that the anti-ferroelectric sample has been saturated at $+V_s$, then this corresponds to point M on the PE loop (Fig. 1 (A)). Lowering the voltage brings the system at point N, which corresponds to a quasi-remanent state of the FE1. Let us introduce the quasi-remanent states $+P_R^{ij}$, where "i" indicates a digital "0" or "1"state and "j" is the sublattice index "1" or "2". Under this convention, point N corresponds then to $+P_R^{01}$. This occurs at a positive reversal voltage called $+V_R$. Continuing to lower the applied voltage, we reach point O at zero applied voltage, where the two sublattices are fully compensated and total polarization is zero. Reversing the applied voltage to negative values, we reach the quasi-remanent state of FE2 at point P, $-P_R^{12}$, corresponding to the reversal voltage $-V_R$. Lowering the voltage further, a negative saturation is reached at point Q corresponding to $-V_s$. Returning to zero voltage, we pass again $-V_R$ reversal voltage, except that this time a different quasi-remanent polarization state of FE2 is observed at point R, $-P_R^{02}$. When the applied voltage is zero, the system returns back to zero polarization state at point O. Ramping up the positive voltage to $+V_R$, the FE1 reaches another quasi-remanent polarization state corresponding to point T and value $+P_R^{11}$. The loop closes back at $+V_s$, point M (Fig. 1(A)). As shown in Fig. 1 (A), there are four possible quasi-remanent memory states, two for each ferroelectric sublattice. The data write operation is the same as for FRAM, simply achieved by applying $+/-V_s$. However, because of the double hysteresis of the anti-ferroelectric, $+V_s$ write operation results in encoding a memory state FE1, $+P_R^{01}$ or simply 01 and a memory state in FE2, $-P_R^{12}$, or simply 12. Similarly, a negative write field $-V_s$ results in two additional memory states 11 and 02. It is important to stress that accessing these states requires an applied reversal voltage $+/-V_R$ as shown in Fig. 1 (A). The "write / read" operations

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protocol required to access the four memory states are also represented diagrammatically in Fig. 1 (B) and Table 1.
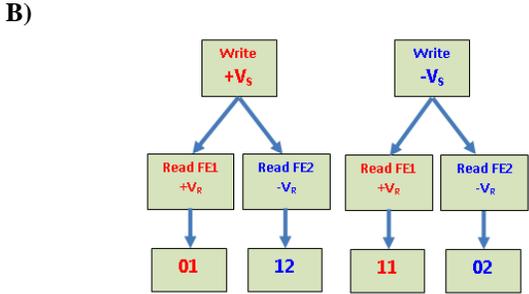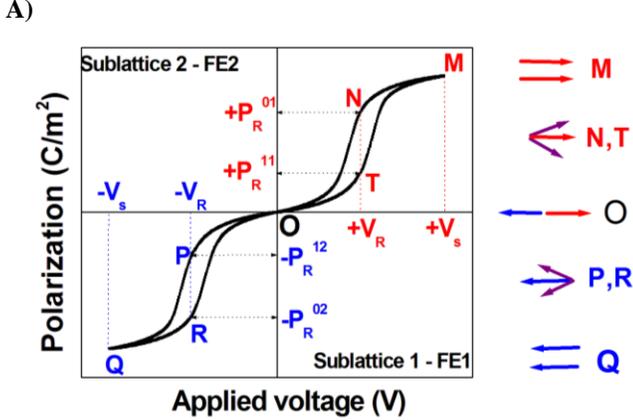
A)

B)

Fig. 1. (A) Polarization versus applied voltage / E field response of a typical anti-ferroelectric material. Key points on the double hysteresis curve are marked, as well as the saturating voltages, reversal voltages and quasi-remanent polarization memory states. The vectors represent diagrammatically the polarization states of the two sublattices at different stages on the hysteresis curve. Red corresponds to positive and blue to negative polarization, respectively. (B) Diagram of the "write / read" protocol of an anti-ferroelectric memory cell with four memory states: 01, 12, 11 and 02, respectively.

In terms of cell structure, a typical FRAM cell contains one capacitor and one access transistor, known as 1T-1C memory cell. This is similar to that of dynamic random access memory (DRAM) architecture, except that the FRAM cell contains a non-linear dielectric capacitor and it requires a third line (the plate line (PL) in addition to the bit line (BL) and the word line (WL). The architecture of the AFRAM memory cell proposed here also consists of one transistor and one anti-ferroelectric capacitor, as shown in Fig. 2. This memory cell architecture is essentially identical to that of the FRAM cells, except that in this case the ferroelectric capacitor is replaced by an anti-ferroelectric capacitor. The write operation works by first raising the BL voltage V_s. The WL voltage is raised to $V_s + V_t$, where the V_t is the threshold voltage of the access transistor. This turns the access transistor ON and results in a voltage V_s across the anti-ferroelectric capacitor. The PL is pulsed to V_s and then pulled back to ground. The WL remains activated until PL is fully pulled down to ground and BL is driven back to zero. Finally the WL is deactivated. The write process results in 01 and 12 memory states written in FE1 and FE2, respectively when $+V_s$ is applied. Similarly, memory states 11 and 02 are achieved in FE1 and FE2, respectively when $-V_s$ is applied (Fig. 1 (B)). These memory states are accessed using read pulses as shown in Fig. 1(B). The possible

permutations of the write / read pulses and the corresponding memory states are shown for clarity in Table 1.

Table 1. AFRAM memory states and the required sequence and polarity of write / read voltages in order to access them.

		AFRAM memory states	
Write	Read	FE1	FE2
+V_S	+V_R	**01**	-
	-V_R	-	**12**
-V_S	+V_R	**11**	-
	-V_R	-	**02**

The possible readout operation of the AFRAM memory cell is based on the "step sensing approach" [3]. The BL is pre-charged to zero volts and the WL is activated. This results in a capacitor divider consisting of C_{AFE} and C_{BL}, between PL and ground. Here C_{AFE} is the anti-ferroelectric capacitance and C_{BL} is the parasitic capacitance of the BL. The PL is raised to the desired reversal voltage V_R, resulting in its division between C_{AFE} and C_{BL}, according to their capacitance.

Depending on the data stored, the capacitance of the anti-ferroelectric capacitor can be approximated by C_{01}, C_{12}, C_{11}, C_{02}, where the indexes correspond to the four possible memory states.
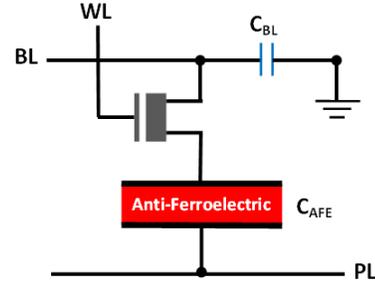

Fig. 2. 1T-1C anti-ferroelectric (AFRAM) memory cell architecture.

From the cell's circuit, it can be easily worked out that the voltage developed on the BL, V_{BL}, can be one of the four values V_{01}, V_{12}, V_{11}, V_{02}, respectively. In generalized form, these are given by:

$$V_{BL} = V_{ij} = \frac{C_{ij}}{C_{ij} + C_{BL}} \cdot V_r \quad (1)$$

where i = 0,1 and j = 1,2. The sense amplifier is then activated to drive the BL to $+V_s$ if the voltage developed on BL was V_{01}, V_{12}, or to $-V_s$ if the BL voltage was V_{11}, V_{02}, respectively. The WL is kept activated until the sense voltage in the BL restores the original data back into the memory cell.

III. EXPERIMENTAL TESTING OF THE AFRAM CONCEPT

In order to experimentally test the AFRAM concept and the "write / read" protocol introduced here, anti-ferroelectric $Pb_{0.99}Nb_{0.02}[(Zr_{0.57}Sn_{0.43})_{0.94}Ti_{0.06}]_{0.98}O_3$ polycrystalline ceramics have been synthesized and measured experimentally. The sample tested here is a disk of 10 mm diameter and 500 µm thickness with code name PNZST 43/6/2. More details of the preparation procedure are given in [10]. Fig. 3 (B) shows a

typical double hysteresis loop corresponding to the PNZST 43/6/2 anti-ferroelectric sample. The four pseudo-remanent memory states are clearly marked on the Polarization versus Voltage loop. From hysteresis loop measurements, we have identified the optimal "write / read" parameters, which are V_s = +/-1.8kV and V_R = +/- 800V. It is important to select the correct "write" voltage so that the ferroelectric sublattices are saturated, but no overall anti-ferroelectric to ferroelectric field induced phase transition is induced. Having these parameters identified, we can experimentally test the potential memory retention of the anti-ferroelectric cell, by implementing the "write / read" protocol as described in Fig. 1(B). The applied "write / read" pulses had trapezoidal form, with the total duration of the pulse being equally split in three: rise time, pulse and fall time. The total duration of the "write" pulse was 3s, out of which the rise time is 1s. For the "read" pulse we used successfully different durations: 500μs, 50ms and 150ms, respectively. These are limited by sample response as well as by the measurement system available to us, which has the shortest "read" pulse available of 250μs. The delay time after read, or the "delay to write" (DTW) time was always fixed to 0.1μs. The "delay after write" was 100s and we successfully demonstrated anti-ferroelectric memory effect after 100s from the write pulse as shown in Fig. 3 (A).
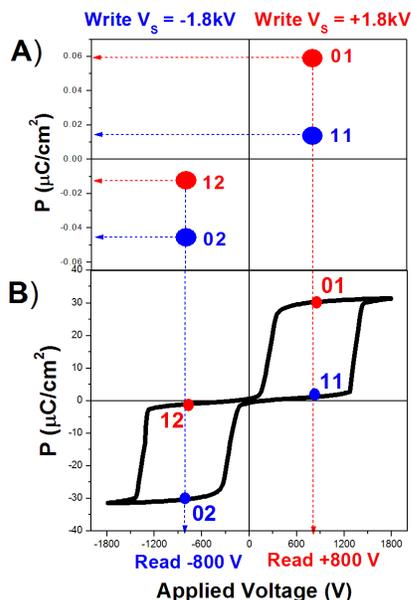

Fig. 3. (A) AFRAM memory retention data taken 100 seconds after the "write" operation. (B) Anti-ferroelectric PNZST 43/6/2 double hysteresis loop at room temperature, using triangular pulse with 0.1Hz frequency. The four pseudo-remanent memory states corresponding to 3(A) are clearly marked on the loop.

Fig. 4 shows an example of the "read" pulse measurement deployed to extract the 02 memory state shown in Fig. 3 (A), where V_s = -1.8kV and V_R = -800V was applied with a pulse duration of 150ms and total duration of 450ms. The same graph shows the polarization response of the sublattice as a function of the pulse duration. The quasi-remanent memory state is extracted from the polarization value at the end of the "read" pulse, which corresponds on our graph to t = 300ms. This technique was deployed to extract experimentally all four memory states of the anti-ferroelectric memory cell, as shown in Fig. 3 (A) and 3 (B), using the four possible permutations of applied pulses: $+V_s/+V_R$, $+V_s/-V_R$, $-V_s/-V_R$ and $-V_s/+V_R$, respectively.
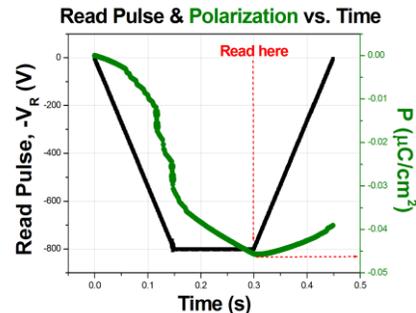

Fig. 4. Example of "read" pulse and polarization response used to extract a quasi-remanent memory state, plotted as a function of time.

Remarkably, the four predicted memory states have been successfully measured experimentally. However, the expected polarization values of the quasi-remanent memory states are much larger than the experimentally measured ones. Fig. 3 (B) shows that states 01 and 02 should read +/-30 μC/cm^2, while states 11 and 12 should read +/-2 μC/cm^2. 100 seconds after the "write" pulse, the extracted polarization memory values are +/- 0.013 and +/-0.045 μC/cm^2, respectively, which are in fact much smaller than expected. This points to a relaxation process and requires further experimental and theoretical investigations, which are beyond the scope of this article. However, despite the obvious signal degradation, a distinguishable and measurable 4-state memory effect in anti-ferroelectrics was clearly demonstrated, indicating the possibility of utilizing anti-ferroelectric materials for future volatile or non-volatile memory chips.

IV. CONCLUSION

We proposed and demonstrated a new random access memory concept based on anti-ferroelectrics (AFRAM). AFRAM has 4 possible memory states, resulting in 2 digital bits stored per cell. By changing the ferroelectric with an anti-ferroelectric capacitor, AFRAM can easily replace the existing FRAM technology. The proposed concept has been tested here using bulk anti-ferroelectric ceramics, which required write and read voltages of ±1.8kV and ±800V, respectively. These correspond to net electric fields of 36 kV/cm and 16 kV/cm, respectively. Based on these values, to make the AFRAM technology suitable for 5V memory chips, a ceramic anti-ferroelectric film of 1.38 μm thickness would be required, which is fully achievable. If the AFRAM capacitor is scaled down to nanometer thickness, extremely low voltages would be enough for its operation, resulting in faster write / read cycles and reduced power consumption. Anti-ferroelectrics are already technologically attractive for various applications [10 - 16], but this letter will stimulate further research and future use of anti-ferroelectric materials to other applications, including random access memories and potentially logic operations, when incorporated into semiconductor devices or multiferroics [17].

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